

1111N (.110" x .110")

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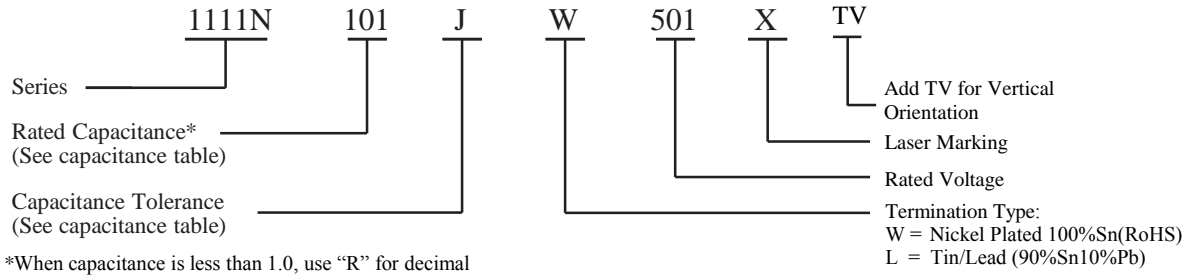


**◆ 1111N Capacitance & Rated Voltage Table**

Cap. pF	Code	Tol.	WVDC V	Cap. pF	Code	Tol.	WVDC V	Cap. pF	Code	Tol.	WVDC V	Cap. pF	Code	Tol.	WVDC V
0.2	0R2	A, B, C, D	500V Code 501 Or 1000V Code 102	3.0	3R0	A, B, C, D	500V Code 501 Or 1000V Code 102	27	270	F, G, J, K	500V Code 501 Or 1000V Code 102	220	221	F, G, J, K	200V Code 201 500V Code 501
0.3	0R3			3.3	3R3			30	300			240	241		
0.4	0R4			3.6	3R6			33	330			270	271		
0.5	0R5			3.9	3R9			36	360			300	301		
0.6	0R6			4.3	4R3			39	390			330	331		
0.7	0R7			4.7	4R7			43	430			360	361		
0.8	0R8			5.1	5R1			47	470			390	391		
0.9	0R9			5.6	5R6			51	510			430	431		
1.0	1R0			6.2	6R2			56	560			470	471		
1.1	1R1			6.8	6R8			62	620			510	511		
1.2	1R2			7.5	7R5			68	680			560	561		
1.3	1R3			8.2	8R2			75	750			620	621		
1.4	1R4			9.1	9R1			82	820			680	681		
1.5	1R5			10	100			91	910			750	751		
1.6	1R6			11	110			100	101			500V Code 501 1000V Code 102	820		
1.7	1R7	12	120	110	111	910	911								
1.8	1R8	13	130	120	121	1000	102								
1.9	1R9	15	150	130	131										
2.0	2R0	16	160	150	151										
2.1	2R1	18	180	160	161										
2.2	2R2	20	200	180	181										
2.4	2R4	22	220	200	201										
2.7	2R7	24	240												

Remark: special capacitance, tolerance and WVDC are available, consult with PASSIVE PLUS.

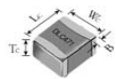
◆ Part Numbering



Capacitance Tolerance								
Code	A	B	C	D	F	G	J	K
Tol.	±0.05pF	±0.1pF	±0.25pF	±0.5pF	±1%	±2%	±5%	±10%

◆ 1111N Chip Dimensions

unit:inch(millimeter)

Series	Term. Code	Type/Outlines	Capacitor Dimensions				Plated Material
			Length Lc	Width Wc	Thickness Tc	Overlap B	
1111N	W		.110 ±.020 ~ -.010 (2.79 +0.51 ~ -.25)	.110 ± .015 (2.79 ± 0.38)	.10 (2.6) Max	0.015 0.024 Max.	Sn/Ni (RoHS)

Also Available in Tin/Lead Termination (90%Sn10%Pb)

### ◆ Design Kits

These capacitors are 100% RoHS. Kits are available that contain 10 (ten) pieces per value; number of values per kit varies, depending on case size and capacitance.

Kit	Description	Values	Tolerances
DKD1111N01	1111N 1.0pF - 10pF	1.0, 1.2, 1.5, 1.8, 2.0, 2.2, 2.4, 2.7, 3.0, 3.3, 3.9, 4.7, 5.6, 6.8, 8.2pF	±.1pF
		10pF	±5%
DKD1111N02	1111N 10pF - 100pF	10, 12, 15, 18, 20, 22, 24, 27, 30, 33, 39, 47, 56, 68, 82, 100pF	±5%
DKD1111N03	1111N 100pF - 1000pF	100, 120, 150, 180, 200, 220, 240, 270, 300, 330, 390, 470, 560, 680, 820, 1000pF	±5%

### ◆ Performance

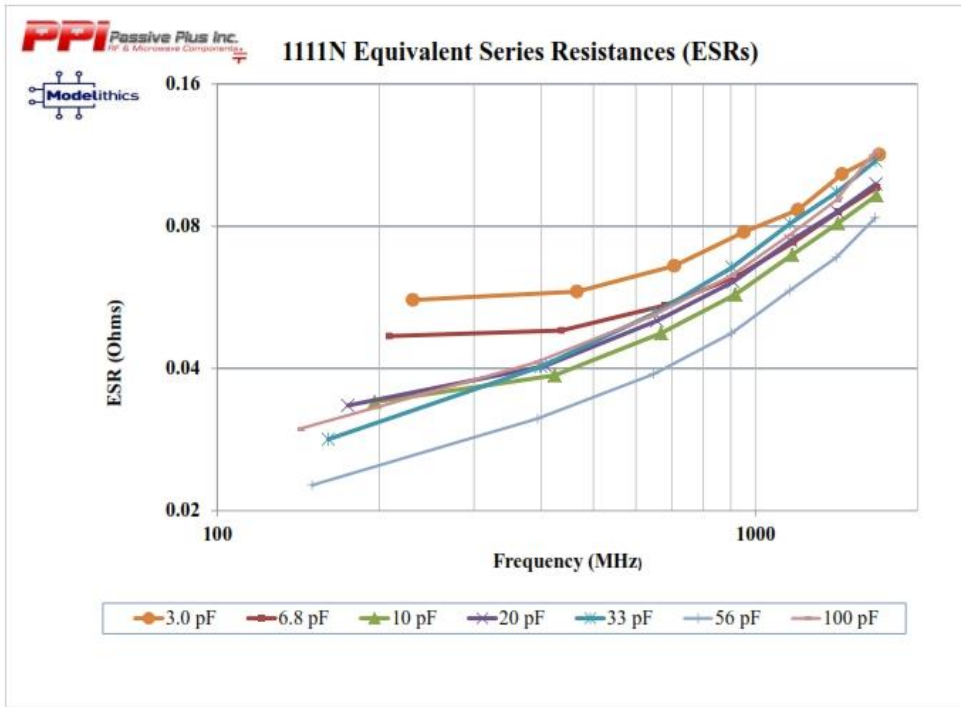
Item	Specifications
Quality Factor (Q)	2,000 min.
Insulation Resistance (IR)	10 <sup>5</sup> Megohms min. @ +25 °C at rated WVDC. 10 <sup>4</sup> Megohms min. @ +125 °C at rated WVDC.
Rated Voltage	See Capacitance Table
Dielectric Withstanding Voltage (DWV)	250% of Voltage for 5 seconds, Rated Voltage ≤ 500VDC 150% of Voltage for 5 seconds, 500VDC < Rated Voltage ≤ 1250VDC 120% of Voltage for 5 seconds, Rated Voltage > 1250VDC
Operating Temperature Range	-55°C to +175°C
Temperature coefficient (TC)	0 ± 30ppm/°C
Capacitance Drift	±0.02% or ±0.02pF, whichever is greater.
Piezoelectric Effects	None

◆ Environmental Tests

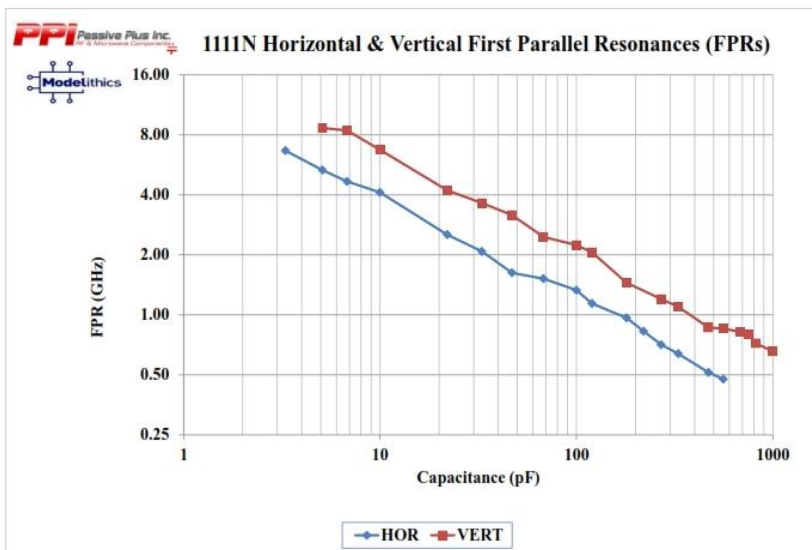
Item	Specifications	Method
Terminal Adhesion	Termination should not pull off. Ceramic should remain undamaged.	Linear pull force exerted on axial leads soldered to each terminal. 2.0lbs.
Resistance To soldering heat	No mechanical damage Capacitance change: -1.0% ~+2.0% Q>500 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	Preheat device to 150°C -180°C for 60 sec. Dip in 260°C ± 5 °C solder for 10 ± 1 sec. Measure after 24 ± 2 hour cooling period.
Thermal Shock	No mechanical damage Capacitance change: ± 0.5% or 0.5pF max Q>500 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 107, Condition A. At the maximum rated temperature (-55°C and 175°C) stay 30 minutes. The time of removing shall not be more than 3 minutes. Perform the five cycles.
Humidity, Steady State	No mechanical damage Capacitance change: ± 0.5% or 0.5pF max. Q>300 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 106.
Low Voltage Humidity	No mechanical damage Capacitance change: ± 0.3% or 0.3pF max. Q>300 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 103, Condition A, with 1.5 Volts D.C. applied while subjected to an environment of 85°C with 85% relative humidity for 240 hours minimum.
Life	No mechanical damage Capacitance change: ± 2.0% or 0.5pF max. Q>500 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	MIL-STD-202, Method 108, for 1000 hours, at 175°C. 200% of Voltage for Capacitors, Rated Voltage ≤500VDC 120% of Voltage for Capacitors, 500VDC < Rated Voltage ≤1250VDC 100% of Voltage for Capacitors, Rated Voltage > 1250VDC

◆ 1111N Electrical Performance Curves

ESR vs. Frequency

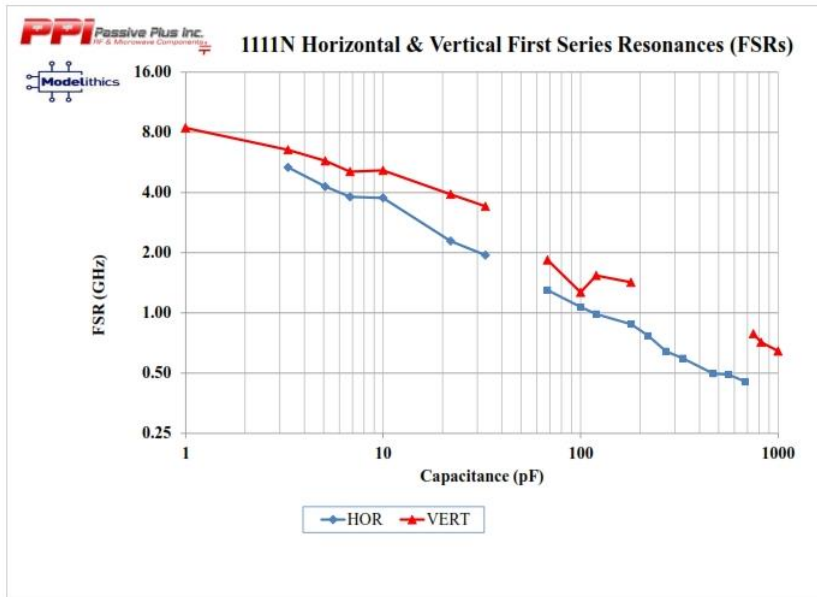


First Parallel Resonant Frequency vs. Capacitance



The First Parallel Resonance, FPR, is defined as the lowest frequency at which a suckout or notch appears in  $|S_{21}|$ . It is generally independent of substrate thickness or dielectric constant, but does depend on capacitor orientation. A horizontal orientation means the capacitor electrode planes are parallel to the plane of the substrate; a vertical orientation means the electrode planes are perpendicular to the substrate.

First Series Resonant Frequency vs. Capacitance



The First Series Resonance, FSR, is defined as the lowest frequency at which the imaginary part of the input impedance,  $\text{Im}[Z_{in}]$ , equals zero. Should  $\text{Im}[Z_{in}]$  or the real part of the input impedance,  $\text{Re}[Z_{in}]$ , not be monotonic with frequency at frequencies lower than those at which  $\text{Im}[Z_{in}] = 0$ , the FSR shall be considered as undefined. FSR is dependent on internal capacitor structure; substrate thickness and dielectric constant; capacitor orientation, as defined alongside the FPR plot; and mounting pad dimensions.

**Definitions and Measurement conditions:**

The definitions on the charts are for a capacitor in a series configuration, i.e., mounted across a gap in a microstrip trace with a 50-Ohm termination. The measurement conditions are: substrate -- Rogers RO4350; substrate dielectric constant = 3.48; horizontal mount substrate thickness (mils) = 55; vertical mount substrate thickness (mils) = 45; gap in microstrip trace, horizontal or vertical mount (mils) = 61.1; horizontal mount microstrip trace width (mils) = 123.7; vertical mount microstrip trace width (mils) = 101.0. **Reference planes at sample edges.**

All data has been derived from electrical models created by Modelithics, Inc., a specialty vendor contracted by PPI. The models are derived from measurements on a large number of parts disposed on several different substrates.

S-Parameters can be found on the PPI Website -- <http://www.passiveplus.com/index.php>

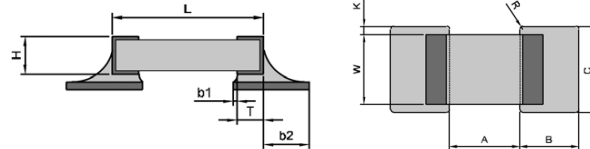
**◆ Recommended Land Pattern Dimensions**

When mounting the capacitor to substrate, it's important to carefully consider that the amount of solder (size of fillet) used has a direct effect upon the capacitor once it's mounted.

- 1) The greater the amount of solder, the greater the stress to the elements. This may cause the substrate to break or crack.
- 2) In the situation where two or more devices are mounted onto a common land, be sure to separate the device into exclusive pads by using soldering resist.

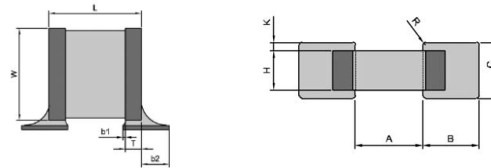
**● Horizontal Mounting**

Orientation	EIA	A	B	C
Horizontal	1111	1.90	1.70	2.90



**● Vertical Mounting**

Orientation	EIA	A	B	C
Vertical	1111	1.90	1.70	2.50



**◆ Tape & Reel Specifications**

Orientation	EIA	A0	B0	K0	W	P0	P1	T	F	QTY Min	QTY/ REEL	Tape Material
Horizontal	1111N	2.92	3.51	2.34	8.00	4.00	4.00	0.254	3.50	500	500	Embossed
Vertical	1111N	2.92	3.51	2.34	8.00	4.00	4.00	0.254	3.50	500	500	Embossed

**● Horizontal Orientation**

**● Vertical Orientation**

